Research on the improvement of IGBT module surge capability

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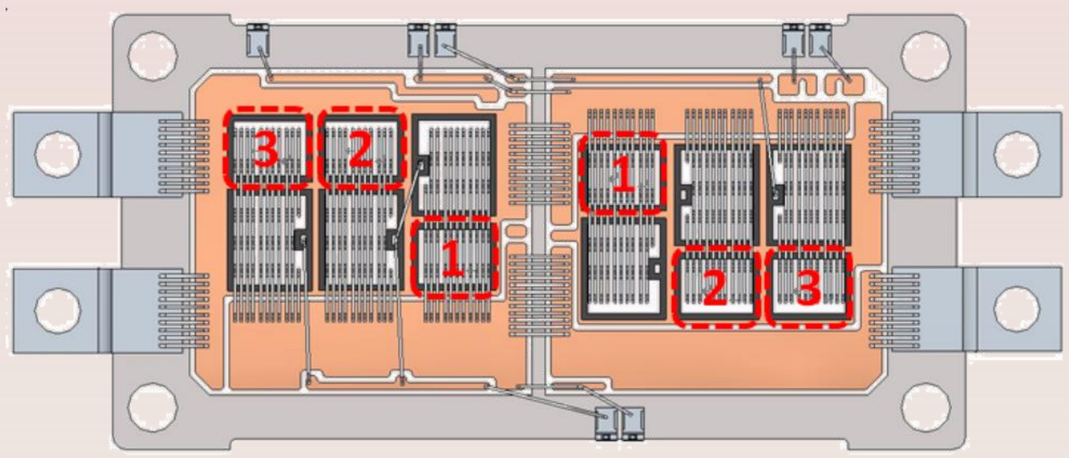
INTRODUCTION

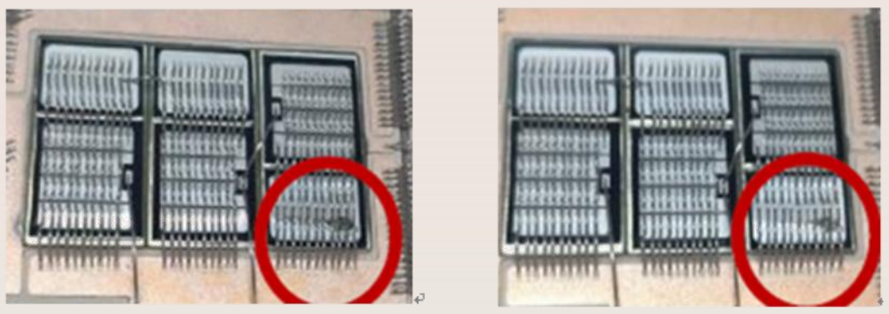
- In practical applications, under abnormal operating conditions such as short circuits, adjacent device damage, or lightning strikes, the current flowing through the Forward Reversed Diode (FRD) is much greater than normal operating conditions, leading to rapid diode temperature rise and ultimately device failure.
- To improve the overall surge capability of the module, this article proposes a method of optimizing the parallel structure of each diode and improving the current sharing characteristics of the device to enhance the overall surge capability.

ANALYSIS OF SURGE FAILURE MECHANISM

- A half sine current with a pulse width of t_p=10ms (corresponding to a frequency of 50 Hz) is used as the test surge current.
- The maximum value of I_{FSM} gradually increases from small to small when the IGBT anti parallel diode passes through a 10 ms sine wave in the forward direction.
- When the reverse cutoff ability of the diode decreases or there is a short circuit, it is determined that the device is faulty. The surge capability is measured by the current before the diode fails, and the integral of I^2t_p is the surge value, also known as I^2t value.
- The average I^2t value of the four modules is 0.95b kA^2s, and all failures are concentrated on FRD 1. After magnification, it was found that the failure points were all located in the bottom right corner of the chip.



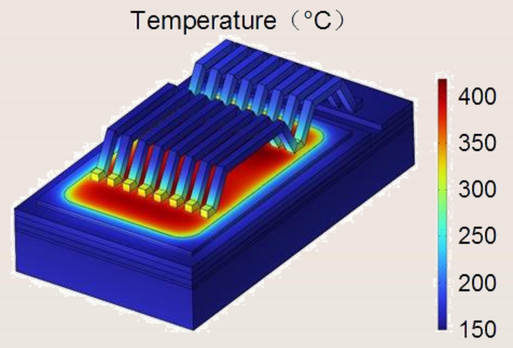
The IGBT module



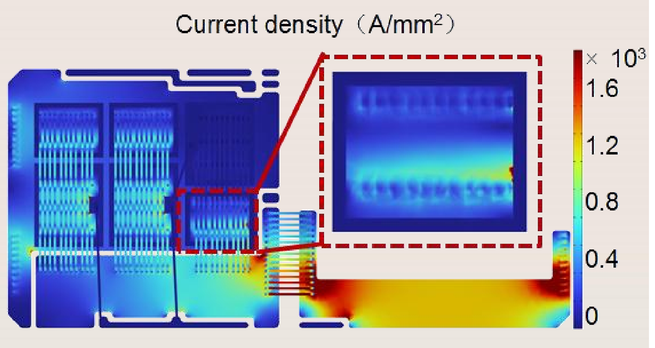
Surge current failure mode

MODULE SURGE CAPABILITY IMPROVEMENT

- In order to improve the I^2t capability of a single chip, three schemes with different number of bonding wires and bonding points are designed.
- Conduct electro-thermal coupling analysis on a single chip model using finite element analysis software. When t_p= 6ms, the temperature reaches its maximum value and the hot spot appears on the aluminum layer next to the bonding point.
- The maximum current density on each chip is used to measure the current of the chip.
- When the current density distribution of the parallel chip is roughly the same, the current sharing performance of the module is better.
- The maximum current density positions of both the upper and lower arms are located at chip 1. Taking the lower arm as an example, extract the current density cloud map of chip 1.
- To improve the current sharing ability of parallel FRDs, increase the current path of chip 1 to make it as consistent as possible with chips 2 and 3. Slot the substrate under chip 1 and extend the bonding wire in two directions to improve the module's current sharing ability.



Temperature profile @ t_p=6ms



Module current density profile

RESULT AND DISCUSSION

- The chip failure position after the surge test as shown. Three FRD chips fail at the same time, indicating that the module has good current sharing capacity.
- The module can effectively improve the surge capacity by improving the current sharing ability of the parallel chip surface.
- Ultimately, the module's surge capability ability is increased by 49.1%.

Surge current failure mode of the selected module